CLAIMS

WHAT IS CLAIMED:

1.   A method comprising:

      forming a gate dielectric above a surface of the substrate;

5   forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region; and

      forming a dopant-depleted-poly region in the edge region of the doped-poly gate structure adjacent the gate dielectric.

10 2.   The method of claim 1, wherein forming the dopant-depleted-poly region includes implanting a counter-dopant into the edge region of the doped-poly gate structure adjacent the gate dielectric.

3.   The method of claim 2, the method further comprising:

15   implanting the counter-dopant at an angle α with respect to a direction perpendicular to the surface, wherein the angle α is in a range of about 7°-45°;

      rotating the substrate through at least one of approximately 90° (approximately π/2 radians), approximately 180° (approximately π radians), and

20   approximately 270° (approximately 3π/2 radians); and

      implanting the counter-dopant at the angle α with respect to the direction perpendicular to the surface.

4.   The method of claim 1, the method further comprising:

forming a photoresist mask defining a source/drain extension (SDE) adjacent
the doped-poly gate structure.

5.   The method of claim 2, the method further comprising:

5   forming a photoresist mask defining a source/drain extension (SDE) adjacent
the doped-poly gate structure.

6.   The method of claim 3, the method further comprising:

forming a photoresist mask defining a source/drain extension (SDE) adjacent
10   the doped-poly gate structure.

7.   The method of claim 1, wherein forming the dopant-depleted-poly region
includes depleting the edge region of the doped-poly gate structure adjacent the gate
dielectric by forming depleting dielectric spacers adjacent the doped-poly gate structure.

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8.   The method of claim 2, wherein implanting the counter-dopant into the edge
region of the doped-poly gate structure includes implanting one of phosphorus, arsenic, boron
and boron fluoride into the edge region of the doped-poly gate structure, a dose of the one of
phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×10^{14} ions/cm^2 to
20   about 1.0×10^{15} ions/cm^2 at an implant energy ranging from about 0.2-5 keV.

9.   The method of claim 3, wherein implanting the counter-dopant into the edge
region of the doped-poly gate structure includes implanting one of phosphorus, arsenic, boron
and boron fluoride into the edge region of the doped-poly gate structure, a dose of the one of

phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×10^{14} ions/cm^2 to about 1.0×10^{15} ions/cm^2 at an implant energy ranging from about 0.2-5 keV.

10.   The method of claim 1, wherein forming the dopant-depleted-poly region in the edge region of the doped-poly gate structure includes forming the dopant-depleted-poly region to have a depth from the edge of the doped-poly gate structure, the depth of the dopant-depleted-poly region ranging from about 50 Å-100 Å.

11.   A method comprising:

forming a gate dielectric above a surface of the substrate;

forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region;

forming a source/drain extension (SDE) adjacent the doped-poly gate structure; and

forming a dopant-depleted-poly region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a dopant-depleted-SDE region in the substrate under the edge region of the doped-poly gate structure.

12.   The method of claim 11, wherein forming the dopant-depleted-poly region includes implanting a counter-dopant into the edge region of the doped-poly gate structure adjacent the gate dielectric, and forming the dopant-depleted-SDE region includes implanting the counter-dopant into the substrate under the edge region of the doped-poly gate structure.

13.   The method of claim 12, the method further comprising:

implanting the counter-dopant at an angle α with respect to a direction perpendicular to the surface, wherein the angle α is in a range of about 7°-45°;

rotating the substrate through at least one of approximately 90° (approximately π/2 radians), approximately 180° (approximately π radians), and approximately 270° (approximately 3π/2 radians); and

implanting the counter-dopant at the angle α with respect to the direction perpendicular to the surface.

14. The method of claim 11, the method further comprising:

forming a photoresist mask defining the SDE adjacent the doped-poly gate structure.

15. The method of claim 12, the method further comprising:

forming a photoresist mask defining the SDE adjacent the doped-poly gate structure.

16. The method of claim 13, the method further comprising:

forming a photoresist mask defining the SDE adjacent the doped-poly gate structure.

17. The method of claim 11, wherein forming the dopant-depleted-poly region includes depleting the edge region of the doped-poly gate structure adjacent the gate dielectric by forming depleting dielectric spacers adjacent the doped-poly gate structure, and forming the dopant-depleted-SDE region includes depleting the SDE in the substrate under

the edge region of the doped-poly gate structure by forming the depleting dielectric spacers above the SDE.

18.   The method of claim 12, wherein implanting the counter-dopant into the edge
5   region of the doped-poly gate structure includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure, and implanting the counter-dopant into the substrate under the edge region of the doped-poly gate structure includes implanting the one of phosphorus, arsenic, boron and boron fluoride into the substrate under the edge region of the doped-poly gate structure, a dose of the one of
10   phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×10^{14} ions/cm^2 to about 1.0×10^{15} ions/cm^2 at an implant energy ranging from about 0.2-5 keV.

19.   The method of claim 13, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure includes implanting one of phosphorus, arsenic, boron
15   and boron fluoride into the edge region of the doped-poly gate structure, and implanting the counter-dopant into the substrate under the edge region of the doped-poly gate structure includes implanting the one of phosphorus, arsenic, boron and boron fluoride into the substrate under the edge region of the doped-poly gate structure, a dose of the one of phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×10^{14} ions/cm^2 to
20   about 1.0×10^{15} ions/cm^2 at an implant energy ranging from about 0.2-5 keV.

20.   The method of claim 11, wherein forming the dopant-depleted-poly region in the edge region of the doped-poly gate structure includes forming the dopant-depleted-poly region to have a first depth from the edge of the doped-poly gate structure, the first depth
25   ranging from about 50 Å-100 Å, and forming the dopant-depleted-SDE region in the

substrate under the edge region of the doped-poly gate structure includes forming the dopant-depleted-SDE region to have a second depth from the surface of the substrate, the second depth ranging from about 50 Å-100 Å.

5   21.   An MOS transistor having a reduced Miller capacitance, the MOS transistor formed by a method comprising:

    forming a gate dielectric above a surface of the substrate;

    forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region; and

10   forming a dopant-depleted-poly region in the edge region of the doped-poly gate structure adjacent the gate dielectric.

        22.   The MOS transistor of claim 21, wherein forming the dopant-depleted-poly region includes implanting a counter-dopant into the edge region of the doped-poly gate 15   structure adjacent the gate dielectric.

        23.   The MOS transistor of claim 22, the method further comprising:

    implanting the counter-dopant at an angle α with respect to a direction perpendicular to the surface, wherein the angle α is in a range of 20   about 7°-45°;

    rotating the substrate through at least one of approximately 90° (approximately $\pi/2$ radians), approximately 180° (approximately π radians), and approximately 270° (approximately $3\pi/2$ radians); and

    implanting the counter-dopant at the angle α with respect to the direction 25   perpendicular to the surface.

24.   The MOS transistor of claim 21, the method further comprising:

forming a photoresist mask defining a source/drain extension (SDE) adjacent

the doped-poly gate structure.

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25.   The MOS transistor of claim 22, the method further comprising:

forming a photoresist mask defining a source/drain extension (SDE) adjacent

the doped-poly gate structure.

10   26.   The MOS transistor of claim 23, the method further comprising:

forming a photoresist mask defining a source/drain extension (SDE) adjacent

the doped-poly gate structure.

27.   The MOS transistor of claim 21, wherein forming the dopant-depleted-poly

15   region includes depleting the edge region of the doped-poly gate structure adjacent the gate

dielectric by forming depleting dielectric spacers adjacent the doped-poly gate structure.

28.   The MOS transistor of claim 22, wherein implanting the counter-dopant into

the edge region of the doped-poly gate structure includes implanting one of phosphorus,

20   arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure, a

dose of the one of phosphorus, arsenic, boron and boron fluoride ranging from

about 1.0×10^{14} ions/cm^2 to about 1.0×10^{15} ions/cm^2 at an implant energy ranging from

about 0.2-5 keV.

29. The MOS transistor of claim 23, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure, a dose of the one of phosphorus, arsenic, boron and boron fluoride ranging from

5   about 1.0×10^{14} ions/cm^2 to about 1.0×10^{15} ions/cm^2 at an implant energy ranging from about 0.2-5 keV.

30. The MOS transistor of claim 21, wherein forming the dopant-depleted-poly region in the edge region of the doped-poly gate structure includes forming the

10   dopant-depleted-poly region to have a depth from an edge of the doped-poly gate structure, the depth of the dopant-depleted-poly region ranging from about 50 Å-100 Å.

31. An MOS transistor having a reduced Miller capacitance, the MOS transistor formed by a method comprising:

15   forming a gate dielectric above a surface of the substrate;

             forming a doped-poly gate structure above the gate dielectric, the doped-poly
                  gate structure having an edge region;

             forming a source/drain extension (SDE) adjacent the doped-poly gate
                  structure; and

20   forming a dopant-depleted-poly region in the edge region of the doped-poly
                  gate structure adjacent the gate dielectric and a dopant-depleted-SDE
                  region in the substrate under the edge region of the doped-poly gate
                  structure.

32.   The MOS transistor of claim 31, wherein forming the dopant-depleted-poly region includes implanting a counter-dopant into the edge region of the doped-poly gate structure adjacent the gate dielectric, and forming the dopant-depleted-SDE region includes implanting the counter-dopant into the substrate under the edge region of the doped-poly gate

5   structure, reducing the Miller capacitance of the edge region of the doped-poly gate structure of the MOS transistor.

33.   The MOS transistor of claim 32, the method further comprising:

implanting the counter-dopant at an angle α with respect to a direction

10   perpendicular to the surface, wherein the angle α is in a range of about 7°-45°;

rotating the substrate through at least one of approximately 90° (approximately $\pi/2$ radians), approximately 180° (approximately π radians), and approximately 270° (approximately $3\pi/2$ radians); and

15   implanting the counter-dopant at the angle α with respect to the direction perpendicular to the surface.

34.   The MOS transistor of claim 31, the method further comprising:

forming a photoresist mask defining the SDE adjacent the doped-poly gate

20   structure.

35.   The MOS transistor of claim 32, the method further comprising:

forming a photoresist mask defining the SDE adjacent the doped-poly gate

structure.

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36.   The MOS transistor of claim 33, the method further comprising:

forming a photoresist mask defining the SDE adjacent the doped-poly gate structure.

5   37.   The MOS transistor of claim 31, wherein forming the dopant-depleted-poly region includes depleting the edge region of the doped-poly gate structure adjacent the gate dielectric by forming depleting dielectric spacers adjacent the doped-poly gate structure, and forming the dopant-depleted-SDE region includes depleting the SDE in the substrate under the edge region of the doped-poly gate structure by forming the depleting dielectric spacers 10 above the SDE.

38.   The MOS transistor of claim 32, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure, and 15 implanting the counter-dopant into the substrate under the edge region of the doped-poly gate structure includes implanting the one of phosphorus, arsenic, boron and boron fluoride into the substrate under the edge region of the doped-poly gate structure, a dose of the one of phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×10^{14} ions/cm^2 to about 1.0×10^{15} ions/cm^2 at an implant energy ranging from about 0.2-5 keV.

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39.   The MOS transistor of claim 33, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure, and implanting the counter-dopant into the substrate under the edge region of the doped-poly gate 25 structure includes implanting the one of phosphorus, arsenic, boron and boron fluoride into

the substrate under the edge region of the doped-poly gate structure, a dose of the one of phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×10^{14} ions/cm^2 to about 1.0×10^{15} ions/cm^2 at an implant energy ranging from about 0.2-5 keV.

5   40.   The MOS transistor of claim 31, wherein forming the dopant-depleted-poly region in the edge region of the doped-poly gate structure includes forming the dopant-depleted-poly region to have a first depth from the edge of the doped-poly gate structure, the first depth ranging from about 50 Å-100 Å, and forming the dopant-depleted-SDE region in the substrate under the edge region of the doped-poly gate structure includes forming the dopant-depleted-SDE region to have a second depth from the surface of the substrate, the second depth ranging from about 50 Å-100 Å.

     41.   An MOS transistor comprising:

         a gate dielectric above a surface of a substrate;

15   a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge and an edge region; and

         a dopant-depleted-poly region in the edge region of the doped-poly gate structure adjacent the gate dielectric.

20   42.   The MOS transistor of claim 41, wherein the dopant-depleted-poly region has a depth from the edge of the doped-poly gate structure, the depth of the dopant-depleted-poly region ranging from about 50 Å-100 Å.

43.   The MOS transistor of claim 41, wherein the MOS transistor has a reduced Miller capacitance in the edge region of the doped-poly gate structure of the MOS transistor due to the dopant-depleted-poly region.

5   44.   An MOS transistor comprising:

a gate dielectric above a surface of a substrate;

a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge and an edge region;

a source/drain extension (SDE) adjacent the doped-poly gate structure;

10   a dopant-depleted-poly region in the edge region of the doped-poly gate structure adjacent the gate dielectric; and

a dopant-depleted-SDE region in the substrate under the edge region of the doped-poly gate structure.

15   45.   The MOS transistor of claim 44, wherein the dopant-depleted-poly region has a first depth from the edge of the doped-poly gate structure, the first depth ranging from about 50 Å-100 Å, and the dopant-depleted-SDE region has a second depth from the edge of the doped-poly gate structure, the second depth ranging from about 50 Å-100 Å.

20   46.   The MOS transistor of claim 44, wherein the MOS transistor has a reduced Miller capacitance in the edge region of the doped-poly gate structure of the MOS transistor due to the dopant-depleted-poly region and the dopant-depleted-SDE region.